BelaSigna 300

Audio Processor for Portable Communication Devices

Introduction

BelaSigna® 300 is a DSP−based mixed−signal audio processing system that delivers superior audio clarity without compromising size or battery life. The processor is specifically designed for monaural portable communication devices requiring high performance audio processing capabilities and programming flexibility when form−factor and power consumption are key design constraints.

The efficient dual−MAC 24−bit CFX DSP core, together with the HEAR configurable accelerator signal processing engine, high speed debugging interface, advanced algorithm security system, state−of−the−art analog front end, Class D output stage and much more, constitute an entire system on a single chip, which enables manufacturers to create a range of advanced and unique products. The system features a high level of instructional parallelism, providing highly efficient computing capability. It can simultaneously execute multiple advanced adaptive noise reduction and echo cancellation algorithms, and uses an asymmetric dual−core patented architecture to allow for more processing in fewer clock cycles, resulting in reduced power consumption.

BelaSigna 300 is supported by a comprehensive suite of development tools, hands−on training, full technical support and a network of solution partners offering software and engineering services to help speed product design and shorten time to market.

Key Features

- **Flexible DSP−based System:** a complete DSP−based, mixed−signal audio system consisting of the CFX core, a fully programmable, highly cycle−efficient, dual−Harvard architecture 24−bit DSP utilizing explicit parallelism; the HEAR configurable accelerator for optimized signal processing; and an efficient input/output controller (IOC) along with a full complement of peripherals and interfaces, which optimize the architecture for audio processing at extremely low power consumption
- **Ultra−low−power:** typically 1−5 mA
- **Excellent Audio Fidelity:** up to 110 dB input dynamic range, exceptionally low system noise and low group delay
- **Miniature Form Factor:** available in a miniature 3.63 mm x 2.68 mm x 0.92 mm (including solder balls) WLCSP package.
- **Multiple Audio Input Sources:** four input channels from five input sources (depends on package selection) can be used simultaneously for multiple microphones or direct analog audio inputs
- **Full Range of Configurable Interfaces:** including a fast I^2C−based interface for download, debug and general communication, a highly configurable PCM interface to stream data into and out of the device, a high−speed UART, an SPI port and 5 GPIOs

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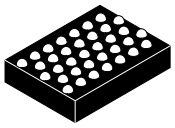

WLCSP−35
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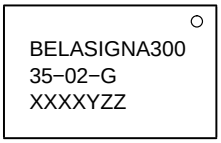
CASE 567AG

MARKING DIAGRAM



BELASIGNA300 = Device Code
35 = Number of Balls
02 = Revision of Die
G = Pb−Free
XXXX = Date Code
Y = Assembly Plant Identifier (May be Two Characters)
ZZ = Traceability Code

ORDERING INFORMATION

Device	Package	Shipping†
B300W35A109XXG	WLCSP (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

- **Integrated A/D Converters and Powered Output:** minimize need for external components
- **Flexible Clocking Architecture:** supports speeds up to 40 MHz
- **“Smart” Power Management:** including low current standby mode requiring only 0.06 mA
- **Diverse Memory Architecture:** 4864x48−bit words of shared memory between the CFX core and the HEAR accelerator plus 8−Kword DSP core data memory, 12−Kwords of 32−bit DSP core program memory as well as other memory banks
- **Data Security:** sensitive program data can be encrypted for storage in external NVRAM to prevent unauthorized parties from gaining access to proprietary software intellectual property, 128−bit AES encryption
- **Development Tools:** interface hardware with USB support as well as a full IDE that can be used for every step of program development including testing and debugging
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Contents

Figures and Data

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Voltage at any input pin	−0.3	2.0	V
Operating supply voltage (Note 1)	0.9	2.0	V
Operating temperature range (Note 2)	−40	85	°C
Storage temperature range (Note 3)	−55	85	°C
Caution: Class 2 ESD Sensitivity, JESD22−A114−B (2000 V)			

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Functional operation only guaranteed below 0°C for digital core (VDDC) and system voltages above 1.0 V.
2. Parameters may exceed listed tolerances when out of the temperature range 0 to 50°C.
3. Extended range −55 to 125°C for storage temperature is under qualification.

Electrical Performance Specifications

The tests were performed at 20°C with a clean 1.8 V supply voltage. BelaSigna 300 was running in low voltage mode (VDDC = 1.2 V). The system clock (SYS_CLK) was set to 5.12 MHz and the sampling frequency is 16 kHz unless otherwise noted.

Parameters marked as screened are tested on each chip. Other parameters are qualified but not tested on every part.

Table 2. ELECTRICAL SPECIFICATIONS

Description	Symbol	Conditions	Min	Typ	Max	Units	Screened
OVERALL							
Supply voltage	V_{BAT}	The WLCSP package option will not operate properly below 1.8 V if it relies on an external EEPROM powered by VBAT.	0.9	1.8	2.0	V	√
Current consumption	I_{BAT}	Filterbank, 100% CFX usage, 5.12 MHz, 16 kHz Ambient room temperature	−	750	−	μA	√
		WDRC, VBAT = 1.8 V Excludes output drive current Ambient room temperature	−	600	−	μA	√
		AEC, VBAT = 1.8 V Excludes output drive current Ambient room temperature	−	2.1	−	mA	√
		Theoretical maximum Excludes output drive current Ambient room temperature	−	10	−	mA	
		Deep Sleep current Ambient room temperature, VBAT = 1.25 V	−	26	40	μA	
		Deep Sleep current Ambient room temperature, VBAT = 1.8 V	−	62	160	μA	√
VREG (1 μF External Capacitor)							
Regulated voltage output	V_{REG}		0.95	1.00	1.05	V	√
Regulator PSRR	V_{REG_PSRR}	1 kHz	50	55	−	dB	
Load current	I_{LOAD}		−	−	2	mA	
Load regulation	$LOAD_{REG}$		−	6.1	6.5	mV/mA	√
Line regulation	$LINE_{REG}$		−	2	5	mV/V	
VDBL (1 μF External Capacitor)							
Regulated doubled voltage output	VDBL		1.9	2.0	2.1	V	√
Regulator PSRR	$VDBL_{PSRR}$	1 kHz	35	41	−	dB	
Load current	I_{LOAD}		−	−	2.5	mA	

Table 2. ELECTRICAL SPECIFICATIONS (continued)

Description	Symbol	Conditions	Min	Typ	Max	Units	Screened
VDBL (1 μF External Capacitor)							
Load regulation	$LOAD_{REG}$		−	7	10	mV/mA	√
Line regulation	$LINE_{REG}$		−	10	20	mV/V	
VDDC (1 μF External Capacitor)							
Digital supply voltage output	VDDC	Configured by a control register	0.79	0.95	1.25	V	√
VDDC output level adjustment	$VDDC_{STEP}$		27	29	31	mV	
Regulator PSRR	$VDDC_{PSRR}$	1 kHz	25	25.5	26	dB	
Load current	I_{LOAD}		−	−	3.5	mA	
Load regulation	$LOAD_{REG}$		−	3	12	mV/mA	√
Line regulation	$LINE_{REG}$		−	3	8	mV/V	
POWER−ON−RESET (POR)							
POR startup voltage	$VDDC_{STARTUP}$		0.775	0.803	0.837	V	
POR shutdown voltage	$VDDC_{SHUTDOWN}$		0.755	0.784	0.821	V	
POR hysteresis	$POR_{HYSTERESIS}$		13.8	19.1	22.0	mV	
POR duration	T_{POR}		11.0	11.6	12.3	ms	
INPUT STAGE							
Analog input voltage	V_{IN}		0	−	2	V	
Preamplifier gain tolerance	PAG	1 kHz	−1	0	1	dB	√
Input impedance	R_{IN}	0 dB preamplifer gain	−	239	−	kΩ	
		Non−zero preamplifier gains	550	578	615	kΩ	√
Input referred noise	IN_{IRN}	Unweighted, 100 Hz to 10 kHz BW Preamplifier setting: 0 dB 12 dB 15 dB 18 dB 21 dB 24 dB 27 dB 30 dB	 − − − − − − − −	 39 10 7 6 4.5 4 3.5 3	 50 12 9 8 5.5 5 4.5 4	μVrms	√
Input dynamic range	IN_{DR}	1 kHz, 20 Hz to 8 kHz BW Preamplifier setting: 0 dB 12 dB 15 dB 18 dB 21 dB 24 dB 27 dB 30 dB	 85 84 84 83 82 81 80 78	 89 88 88 87 86 85 83 81	 − − − − − − − −	dB	
Input peak THD+N	IN_{THDN}	Any valid preamplifier gain, 1 kHz	−	−70	−63	dB	√
DIRECT DIGITAL OUTPUT							
Maximum load current	I_{DO}	Normal mode	−	−	50	mA	
Output impedance	R_{DO}	Normal mode	−	−	5.5	Ω	
Output dynamic range	DO_{DR}	Unweighted, 100 Hz to 8 kHz BW, mono	92	95	−	dB	

Table 2. ELECTRICAL SPECIFICATIONS (continued)

Description	Symbol	Conditions	Min	Typ	Max	Units	Screened
DIRECT DIGITAL OUTPUT							
Output THD+N	DO_{THDN}	Unweighted, 100 Hz to 22 kHz BW, mono	−	−79	−76	dB	√
Output voltage	DO_{VOUT}		$-V_{BATRCVR}$		$V_{BATRCVR}$	V	
ANTI−ALIASING FILTERS (Input and Output)							
Preamplifier filter cut−off frequency		Preamp not bypassed	−	20	−	kHz	√
Digital anti−aliasing filter cut−off frequency			−	$f_S/2$	−		√
Passband flatness			−1	−	1	dB	
Input stopband attenuation		60 kHz (12 kHz cut−off)	−	60	−	dB	√
LOW−SPEED A/D							
Input voltage		Peak input voltage	0	−	2.0	V	√
INL		From GND to 2*VREG	−	4	10	LSB	
DNL		From GND to 2*VREG	−	−	2	LSB	
Maximum variation over temperature (0°C to 50°C)			−	−	5	LSB	
Sampling frequency		All channels sequentially	−	12.8	−	kHz	
Channel sampling frequency		8 channels	−	1.6	−	kHz	
DIGITAL PADS							
Voltage level for high input	V_{IH}		VBAT * 0.8	−	−	V	√
Voltage level for low input	V_{IL}		−	−	VBAT * 0.2	V	√
Voltage level for high output	V_{OH}	2 mA source current	VDDO * 0.8	−	−	V	√
Voltage level for low output	V_{OL}	2 mA sink current	−	−	VDDO * 0.2	V	√
Input capacitance for digital pads	C_{IN}		−	4	−	pF	
Pull−up resistance for digital input pads	R_{UP_IN}		220	270	320	kΩ	√
Pull−down resistance for digital input pads	R_{DOWN_IN}		220	270	320	kΩ	√
Sample rate tolerance	FS	Sample rate of 16 kHz or 32 kHz	−1	±0	+1	%	
Rise and fall time	Tr, Tf	Digital output pad					
ESD		Human Body Model (HBM)			2	kV	
		Machine Model (MM)			200	V	
		Charged Device Model (CDM)			500	V	
Latch−up		V < GNDC, V > VBAT			200	mA	
OSCILLATION CIRCUITRY							
Internal oscillator frequency	SYS_CLK		0.5	−	10.24	MHz	√
Calibrated internal clock frequency	SYS_CLK		−1	±0	+1	%	√
Internal oscillator jitter		System clock: 1.28 MHz	−	0.4	1	ns	

Table 2. ELECTRICAL SPECIFICATIONS (continued)

Description	Symbol	Conditions	Min	Typ	Max	Units	Screened
OSCILLATION CIRCUITRY							
External oscillator tolerances	EXT_CLK	Duty cycle	45	50	55	%	
		System clock: 30 MHz	−	−	300	ps	
Maximum working frequency	CLK_{MAX}	External clock; VBAT: 1.8 V		−	40	MHz	√
DIGITAL INTERFACES							
I2C baud rate		System clock < 1.6 MHz	−	−	100	kbps	
		System clock > 1.6 MHz	−	−	400	kbps	
General−purpose UART baud rate		System clock ≥ 5.12 MHz	−	1	−	Mbps	

Environmental Characteristics

All BelaSigna 300 parts are Pb−free, RoHS−compliant and Green.

BelaSigna 300 parts are qualified against standards outlined in the following sections.

All BelaSigna 300 parts are Green (RoHS−compliant). Contact ON Semiconductor for supporting documentation.

WLCSP Package Option

The solder ball composition for the WLCSP package is SAC266.

Table 3. PACKAGE−LEVEL QUALIFICATION

Packaging Level	
Moisture sensitivity level	JEDEC Level 1
Thermal cycling test (TCT)	−55°C to 150°C for 500 cycles
Highly accelerated stress test (HAST)	85°C / 85% RH for 1000 hours
High temperature stress test (HTST)	150°C for 1000 hours

Table 4. BOARD−LEVEL QUALIFICATION

Board Level	
Temperature	−40°C to 125°C for 2500 cycles with no failures

Mechanical Information and Circuit Design Guidelines

BelaSigna 300 is available in a 2.68 x 3.63 mm ultra−miniature wafer−level chip scale package (WLCSP).

WLCSP Pin Out

A total of 35 active pins are present on BelaSigna 300. They are organized in a staggered array. A description of these pins is given in Table 5.

Table 5. PAD DESCRIPTIONS

Pad Index	BelaSigna 300 Pad Name	Description	I/O	A/D
A1	GNDRCVR	Ground for output driver	N/A	A
A5	VBATRCVR	Power supply for output stage	I	A
B2	RCVR_HP+	Extra output driver pad for high power mode	O	A
C3	RCVR+	Output from output driver	O	A
A3	RCVR−	Output from output driver	O	A
B4	RCVR_HP−	Extra output driver pad for high power mode	O	A
B6	CAP0	Charge pump capacitor pin 0	N/A	A
C5	CAP1	Charge pump capacitor pin 1	N/A	A
A7	VDBL	Doubled voltage	O	A
B8	VBAT	Power supply	I	A
B10	VREG	Regulated supply voltage	O	A
A9	AGND	Analog ground	N/A	A
A11	AI4	Audio signal input 4	I	A
B12	AI2/LOUT2	Audio signal input 2/output signal from preamp 2	I/O	A
A13	AI1/LOUT1	Audio signal input 1/output signal from preamp 1	I/O	A
B14	AI0/LOUT0	Audio signal input 0/output signal from preamp 0	I/O	A
D14	GPIO[4]/LSAD[4]	General−purpose I/O 4/low speed AD input 4	I/O	A/D
E13	GPIO[3]/LSAD[3]	General−purpose I/O 3/low speed AD input 3	I/O	A/D
C13	GPIO[2]/LSAD[2]	General−purpose I/O 2/low speed AD input 2	I/O	A/D
D12	GPIO[1]/LSAD[1]/UART−RX	General−purpose I/O 1/low speed AD input 1/and UART RX	I/O	A/D
E11	GPIO[0]/UART−TX	General−purpose I/O 0/UART TX	I/O	A/D
C9	GNDC	Digital ground	N/A	A
C11	SDA (I2C)	I2C data	I/O	D
D10	SCL (I2C)	I2C clock	I/O	D
E9	EXT_CLK	External clock input/internal clock output	I/O	D
D8	VDDC	Core logic power	O	A
E7	SPI_CLK	Serial peripheral interface clock	O	D
C7	SPI_SERI	Serial peripheral interface input	I	D
D6	SPI_CS	Serial peripheral interface chip select	O	D
E5	SPI_SERO	Serial peripheral interface output	O	D
D4	PCM_FR	PCM interface frame	I/O	D
E3	PCM_SERI	PCM interface input	I	D
D2	PCM_SERO	PCM interface output	O	D
C1	PCM_CLK	PCM interface clock	I/O	D
E1	Reserved	Reserved		

Assembly / Design Notes

For PCB manufacture with BelaSigna 300, ON Semiconductor recommends solder−on−pad (SoP) surface finish. With SoP, the solder mask opening should be non−solder mask−defined (NSMD) and copper pad geometry will be dictated by the PCB vendor's design requirements.

Alternative surface finishes are ENiG and OSP; volume of screened solder paste (#5) should be less than 0.0008 mm^3. If no pre−screening of solder paste is used, then following conditions must be met:

1. the solder mask opening should be >0.3 mm in diameter,
2. the copper pad will have 0.25 mm diameter, and
3. soldermask thickness should be less than 1 mil thick above the copper surface.

ON Semiconductor can provide BelaSigna 300 WLCSP land pattern CAD files to assist your PCB design upon request.

WLCSP Weight

BelaSigna 300 has an average weight of 0.095 grams.

Recommended Circuit Design Guidelines

BelaSigna 300 is designed to allow both digital and analog processing in a single system. Due to the mixed−signal nature of this system, the careful design of the printed circuit board (PCB) layout is critical to maintain the high audio fidelity of BelaSigna 300. To avoid coupling noise into the audio signal path, keep the digital traces away from the analog traces. To avoid electrical feedback coupling, isolate the input traces from the output traces.

Recommended Ground Design Strategy

The ground plane should be partitioned into two: the analog ground plane (AGND) and the digital ground plane (DGND). These two planes should be connected together at a single point, known as the star point. The star point should be located at the ground terminal of a capacitor on the output of the power regulator as illustrated in Figure 1.

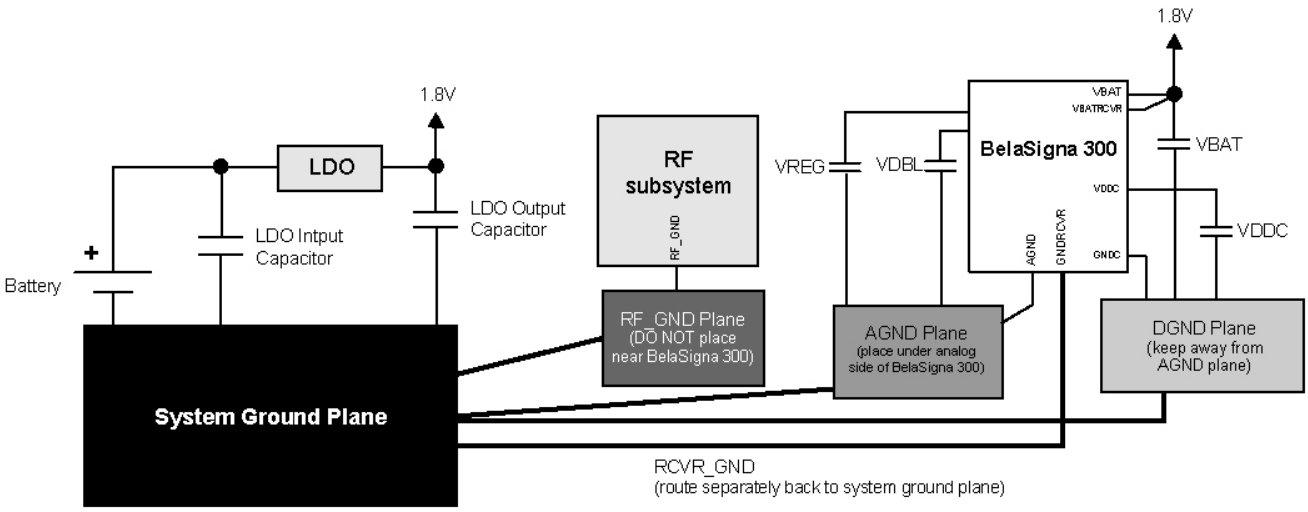


Figure 1. Schematic of Ground Scheme

The DGND plane is used as the ground return for digital circuits and should be placed under digital circuits. The AGND plane should be kept as noise−free as possible. It is used as the ground return for analog circuits and it should surround analog components and pins. It should not be connected to or placed under any noisy circuits such as RF chips, switching supplies or digital pads of BelaSigna 300 itself. Analog ground returns associated with the audio output stage should connect back to the star point on separate individual traces.

For details on which signals require special design consideration, see Table 6 and Table 7.

In some designs, space constraints may make separate ground planes impractical. In this case a star configuration strategy should be used. Each analog ground return should connect to the star point with separate traces.

Internal Power Supplies

Power management circuitry in BelaSigna 300 generates separate digital (VDDC) and analog (VREG, VDBL) regulated supplies. Each supply requires an external decoupling capacitor, even if the supply is not used externally. Decoupling capacitors should be placed as close as possible to the power pads. The VDDC internal regulator is a programmable power supply that allows the selection of the lowest digital supply depending on the clock frequency at which BelaSigna 300 will operate. See the Internal Digital Supply Voltage section for more details on VDDC.

Two other supply pins are also available on BelaSigna 300 (VDDO and VDDO_SPI) which are internally connected to the VBAT pin.

Further details on these critical signals are provided in Table 6. Non−critical signals are outlined in Table 7.

Table 6. CRITICAL SIGNALS

Pin Name	Description	Routing Guideline
VBAT	Power supply	Place 1 μF (min) decoupling capacitor close to pin. Connect negative terminal of capacitor to DGND plane.
VREG, VDBL	Internal regulator for analog sections	Place separate 1 μF decoupling capacitors close to each pin. Connect negative capacitor terminal to AGND. Keep away from digital traces and output traces. VREG may be used to generate microphone bias. VDBL shall not be used to supply external circuitry.
AGND	Analog ground return	Connect to AGND plane.
VDDC	Internal regulator for digital core	Place 10 μF decoupling capacitor close to pin. Connect negative terminal of capacitor to DGND.
GNDC	Digital ground return	Connect to digital ground.
AI0/LOUT0, AI1/LOUT1, AI2/LOUT2	Audio inputs	Keep as short as possible. Keep away from all digital traces and audio outputs. Avoid routing in parallel with other traces. Connect unused inputs to AGND.
RCVR+, RCVR−, RCVR_HP+, RCVR_HP−	Direct digital audio output	Keep away from analog traces, particularly audio inputs. Corresponding traces should be of approximately the same length. Ideally, route lines parallel to each other.
GNDRCVR	Output stage ground return	Connect to star point. Keep away from all analog audio inputs.
EXT_CLK	External clock input / internal clock output	Minimize trace length. Keep away from analog signals. If possible, surround with digital ground.

Table 7. NON−CRITICAL SIGNALS

Pin Name	Description	Routing Guideline
CAP0, CAP1	Internal charge pump − capacitor connection	Place 100 nF capacitor close to pins
SDA, SCL	I2C port	Keep as short as possible
GPIO[3..0]	General−purpose I/O	Not critical
UART_RX, UART_TX	General−purpose UART	Not critical
PCM_FRAME, PCM_CLK, PCM_OUT, PCM_IN	PCM port	Keep away from analog input lines
LSAD[4..1]	Low−speed A/D converters	Not critical
SPI_CLK, SPI_CS, SPI_SERI, SPI_SERO	Serial peripheral interface port Connect to EEPROM	Keep away from analog input lines

Audio Inputs

The audio input traces should be as short as possible. The input impedance of each audio input pad (e.g., AI0, AI1, AI2, AI3, AI4) is high (approximately 500 kΩ); therefore a 10 nF capacitor is sufficient to decouple the DC bias. This capacitor and the internal resistance form a first−order analog high pass filter whose cutoff frequency can be calculated by f_{3dB} (Hz) = 1/(R x C x 2π), which results in ~30 Hz for a 10 nF capacitor. This 10 nF capacitor value applies when the preamplifier is being used, in other words, when a non−unity gain is applied to the signals. When the preamplifier is by−passed, the impedance is reduced; hence, the cut−off frequency of the resulting high−pass filter could be too high. In such a case, the use of a 30−40 nF serial capacitor is recommended. In cases where line−level analog inputs without DC bias are used, the capacitor may be omitted for transparent bass response.

BelaSigna 300 provides microphone power supply (VREG) and ground (AGND). Keep audio input traces strictly away from output traces. A 2.0 V microphone bias might also be provided by the VDBL power supply.

Digital outputs (RCVR) MUST be kept away from microphone inputs to avoid cross−coupling.

Audio Outputs

The audio output traces should be as short as possible. The trace length of RCVR+ and RCVR− should be approximately the same to provide matched impedances.

Recommendation for Unused Pins

The table below shows the recommendation for each pin when they are not used.

Table 8. RECOMMENDATIONS FOR UNUSED PADS

WLCSP Ball Index	BelaSigna 300 Signal Name	Recommended Connection when Not Used
B2	RCVR_HP+	Do not connect
C3	RCVR+	Do not connect
A3	RCVR−	Do not connect
B4	RCVR_HP−	Do not connect
A11	AI4	Connect to AGND
N/A	AI3/LOUT3	Connect to AGND
B12	AI2/LOUT2	Connect to AGND
A13	AI1/LOUT1	Connect to AGND
B14	AI0/LOUT0	Connect to AGND
D14	GPIO[4]/LSAD[4]	Do not connect
E13	GPIO[3]/LSAD[3]	Do not connect
C13	GPIO[2]/LSAD[2]	Do not connect
D12	GPIO[1]/LSAD[1]/UART−RX	Do not connect
E11	GPIO[0]/UART−TX	Do not connect
E9	EXT_CLK	Do not connect
E7	SPI_CLK	Do not connect
C7	SPI_SERI	Do not connect

Table 8. RECOMMENDATIONS FOR UNUSED PADS (continued)

WLCSP Ball Index	BelaSigna 300 Signal Name	Recommended Connection when Not Used
D6	SPI_CS	Do not connect
E5	SPI_SERO	Do not connect
D4	PCM_FR	Do not connect
E3	PCM_SERI	Do not connect
D2	PCM_SERO	Do not connect
C1	PCM_CLK	Do not connect
E1	Reserved	Connect to GND

Architecture Overview

The architecture of BelaSigna 300 is shown in Figure 2.

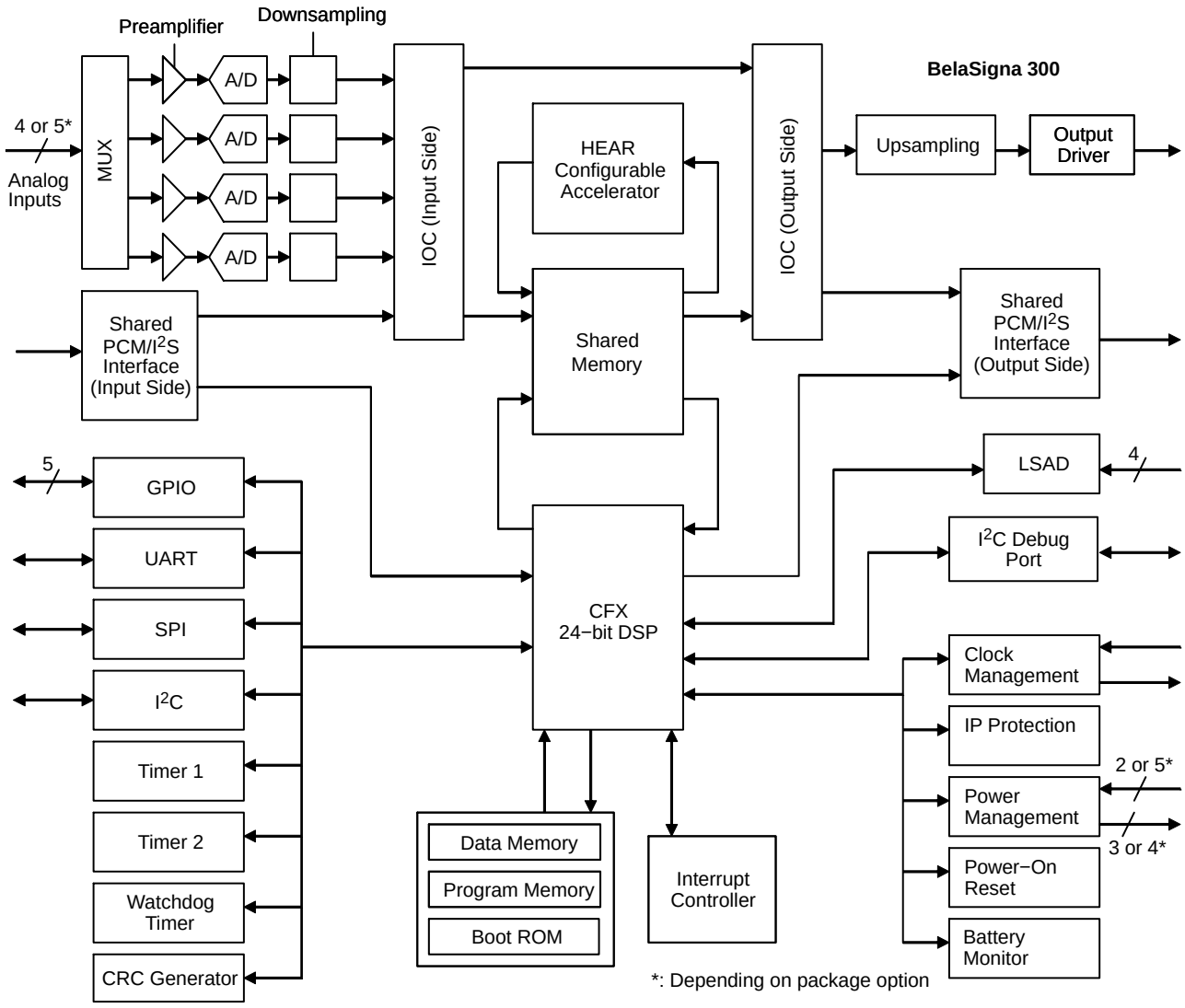


Figure 2. BelaSigna 300 Architecture: A Complete Audio Processing System

CFX DSP Core

The CFX DSP is a user−programmable general−purpose DSP core that uses a 24−bit fixed−point, dual−MAC, dual−Harvard architecture. It is able to perform two MACs, two memory operations and two pointer updates per cycle, making it well−suited to computationally intensive algorithms.

The CFX features:

- Dual−MAC 24−bit load−store DSP core
- Four 56−bit accumulators
- Four 24−bit input registers
- Support for hardware loops nested up to 4 deep
- Combined XY memory space (48−bits wide)
- Dual address generator units
- Wide range of addressing modes:
  - Direct
  - Indirect with post−modification
  - Modulo addressing
  - Bit reverse

CFX DSP Architecture

The CFX architecture encompasses various memory types and sizes, peripherals, interrupt controllers, and interfaces. Figure 3 illustrates the basic architecture of the CFX. The control lines shown exiting the PCU indicate that control signals go from the PCU to essentially all other parts of the CFX.

The CFX employs a parallel instruction set for simultaneous control of multiple computation units. The DSP can execute up to four computation operations in parallel with two data transfers (including rounding and/or saturation as well as complex address updates), while simultaneously changing control flow.

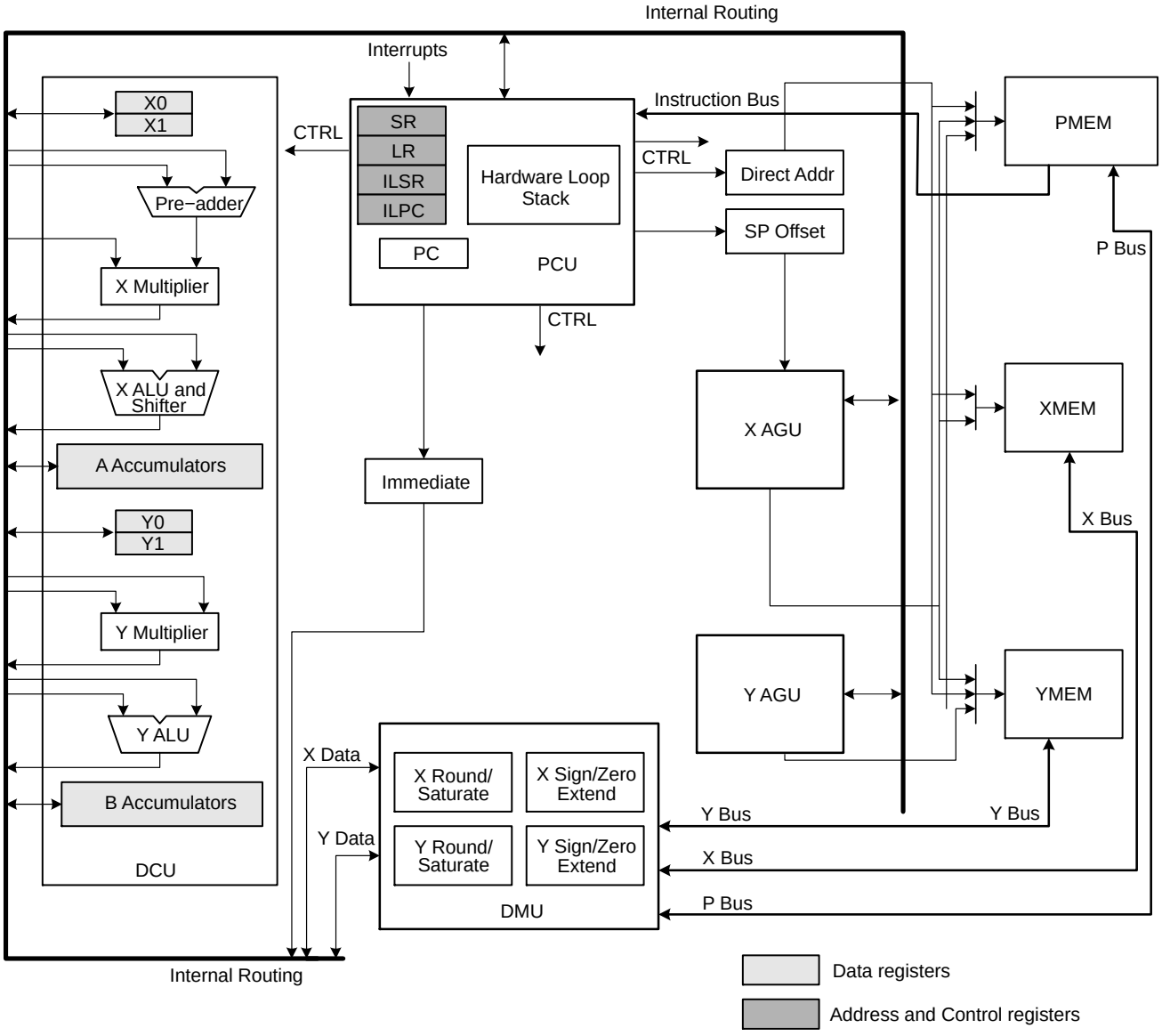


Figure 3. CFX DSP Core Architecture

CFX DSP Instruction Set

Table 9 shows the list of all general CFX instructions and their description. Many instructions have multiple variations not shown in the table. Please refer to the CFX DSP Architecture Manual for more details.

Table 9. CFX SUMMARY INSTRUCTION SET

Instruction	Description
ABS	Calculate the absolute value of a data register or accumulator
ADD	Add values (various combinations of accumulators, pointers and data registers)
ADDMUL	Add two XY data registers, multiply the result by a third XY data register, and store the result in an accumulator
ADDMULADD	Add two XY data registers, multiply the result by a third XY data register, and add the result to an accumulator
ADDMULNEG	Add two XY data registers, multiply the result by a third XY data register, negate the result and store it in an accumulator
ADDMULSUB	Add two XY data registers, multiply the result by a third XY data register, and subtract the result from an accumulator
ADDSH	Add two data registers or accumulators and shift right one bit, storing the result
AND	Perform a bitwise AND operation on the two operands
BITCLR	Clear a bit in the register
BITSET	Set a bit in the register
BITTGL	Toggle a bit in a data register
BITTST	Test a bit in a data register
BREAKPOINT	Halts the DSP for debugging if software breakpoints are enabled through the debug port
CALL	Call a subroutine
CLR	Clear a word of X memory specified by an X pointer, with update
CMP	Compare a data register or accumulator to another data register or accumulator or a value
CMPU	Compare a data register to a value or another data register as unsigned values or compare two accumulators as unsigned values
DIVST	Division step for dividing data register by data register and stores the result to a data register
ENDLOOP	End a hardware loop before the count has reached zero
GOTO	Branch to an address or label
INTERRUPT	Software interrupt
LOAD	Load a register, accumulator or a memory location with another register, accumulator or data
LOG2ABS	Calculate the logarithm base 2 of the absolute value of a data register, storing the result in a data register
LOOP	Loop with a specified count
MAX	Determine the maximum value of two data registers or accumulators and store the result in a data register or accumulator
MIN	Determine the minimum value of two data registers or accumulators and store the result in a data register or accumulator
MOVE	Move a register or accumulator to a register or accumulator
MUL	Multiply two XY data registers, storing the result in an accumulator
MULADD	Multiply two XY data registers, and add the result to an accumulator
MULNEG	Multiply two XY data registers, negate the result and store it in an accumulator
MULSUB	Multiply two XY data registers, and subtract the result from an accumulator
NEG	Negate a data register or accumulator, storing the result in a data register or accumulator
NLOG2ABS	Calculate the logarithm base 2 of the absolute value of a data register, negate the result, and store the result in a data register
NOP	No operation
OR	Perform a bitwise OR operation on two accumulators storing the result in an accumulator or on two data registers or a data register and value, storing the result in a data register
RETURN	Return from a subroutine

Table 9. CFX SUMMARY INSTRUCTION SET (continued)

Instruction	Description
RETURNI	Return from an interrupt
SHLL	Shift a data register left logically
SHRA	Shift a data register right arithmetically
SHRL	Shift a data register right logically
SLEEP	Enter sleep mode and wait for an interrupt and then wake up from sleep mode
STORE	Store data, a register or accumulator in a register, accumulator or memory location
SUB	Subtract two data registers or accumulators, storing the result in a data register or accumulator
SUBMUL	Subtract two XY data registers, multiply the result by a third XY data register, and store the result in an accumulator
SUBMULADD	Subtract two XY data registers, multiply the result by a third XY data register, and add the result to an accumulator
SUBMULNEG	Subtract two XY data registers, multiply the result by a third XY data register, negate the result and store it in an accumulator
SUBMULSUB	Subtract two XY data registers, multiply the result by a third XY data register, and subtract the result from an accumulator
SUBSH	Subtract two data registers or two accumulators and shift right one bit, storing the result in a data register or accumulator
SUBSTEP	Subtract a step register from the corresponding pointer
SWAP	Swap the contents of two data registers, conditionally
XOR	Perform a bitwise XOR operation on two data registers or a data register and a value, storing the result in a data register

HEAR Configurable Accelerator

The HEAR Configurable Accelerator is a highly optimized signal processing engine that is configured through the CFX. It offers high speed, high flexibility and high performance, while maintaining low power consumption. For added computing precision, the HEAR supports block floating point processing. Configuration of the HEAR is performed using the HEAR configuration tool (HCT). For further information on the usage of the HEAR and the HCT, please refer to the HEAR Configurable Accelerator Reference Manual.

The HEAR is optimized for advanced audio algorithms, including but not limited to the following:

- Dynamic range compression
- Directional processing
- Acoustic echo cancellation
- Noise reduction

To provide the ability for these algorithms to be executed efficiently, the HEAR excels at the following:

- Processing using a weighted overlap add (WOLA) filterbank or FFT
- Time domain filtering
- Subband filtering
- Attack/release filtering
- Vector addition/subtraction/multiplication
- Signal statistics (such as average, variance and correlation)

Input/Output Controller (IOC)

The IOC is responsible for the automated data moves of all audio samples transferred in the system. The IOC can manage any system configuration and route the data accordingly. It is an advanced audio DMA unit.

Memory

RAM & ROM

The size and width of each of the RAM and ROM structures are shown in Table 10:

Table 10. RAM AND ROM STRUCTURE

Memory Structure	Data Width	Memory Size
Program memory (ROM)	32	2048
Program memory (RAM)	32	12288
X memory (RAM)	24	6144
Math library LUT (ROM)	24	128
Y memory (RAM)	24	2048

Shared Memories

The shared CFX/HEAR memories include the following:

Table 11. SHARED MEMORIES

Type	Name	Size
Data memory (RAM)	H0MEM, H1MEM, H2MEM, H3MEM, H4MEM, H5MEM	Each 128x48−bit words
FIFO memory (RAM)	AMEM, BMEM	Each 1024x48−bit words
Coefficient memory (RAM)	CMEM, DMEM	Each 1024x48−bit words
Data ROM	SIN/COS LUT	512x48−bit words containing the 512 point sin/cos look up table
Microcode memory (RAM)	MICROCODE_MEM	2048x32−bit words

Memories Structure

Figure 4 shows the system memory structure. The individual blocks are described in the sections that follow.

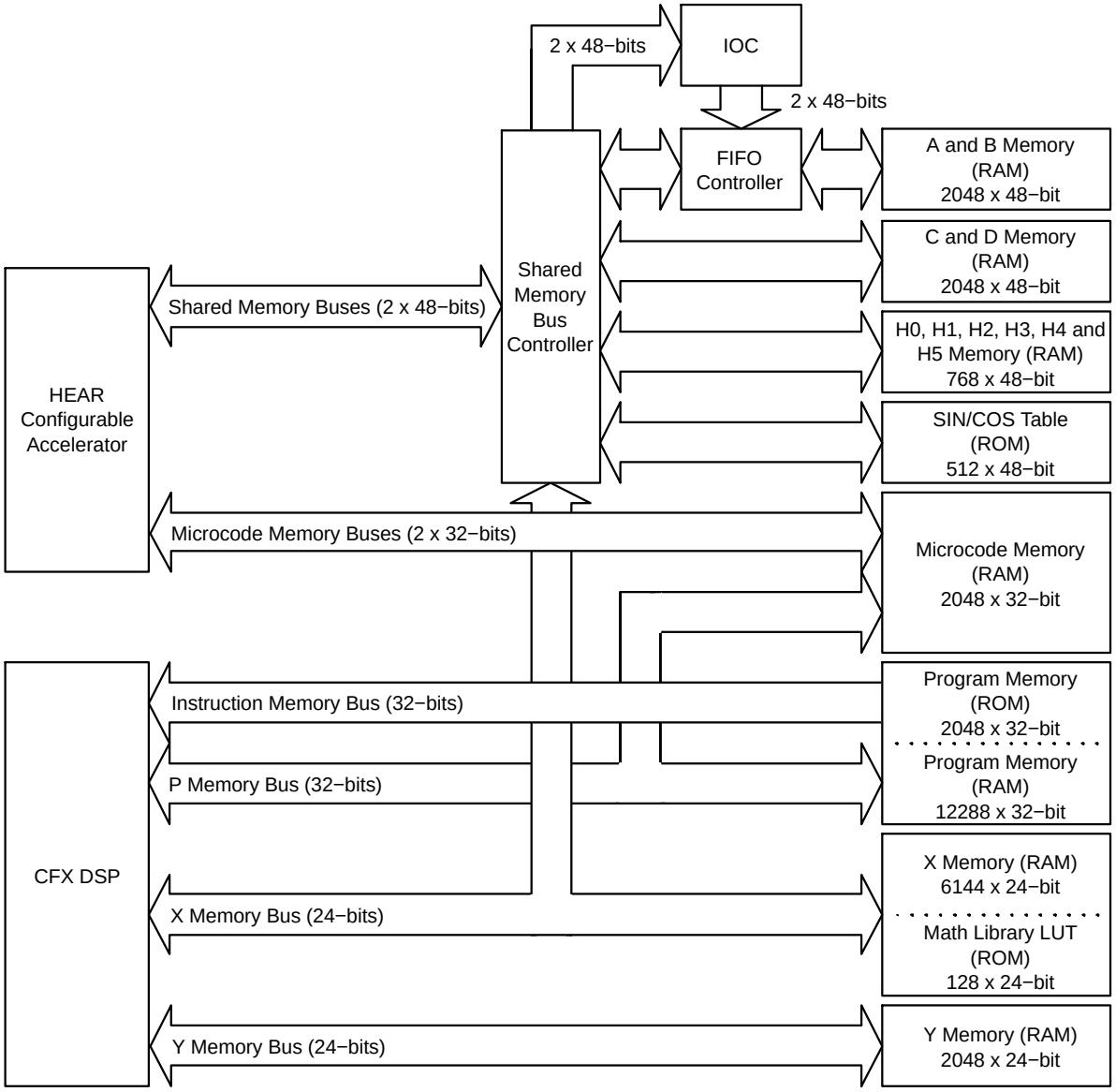


Figure 4. System Memory Architecture

FIFO Controller

The FIFO controller handles the moving of data to and from the FIFOs, after being initially configured. Up to eight FIFOs can be created by the FIFO controller, four in A memory (AMEM) and four in B memory (BMEM). Each FIFO has a block counter that counts the number of samples read or written by the IOC. It creates a dedicated interrupt signal, updates the block counter and updates the FIFO pointers when a new block has been read or written.

Memory Maps

The structure of the XMEM and YMEM address spaces are shown in Figure 5.

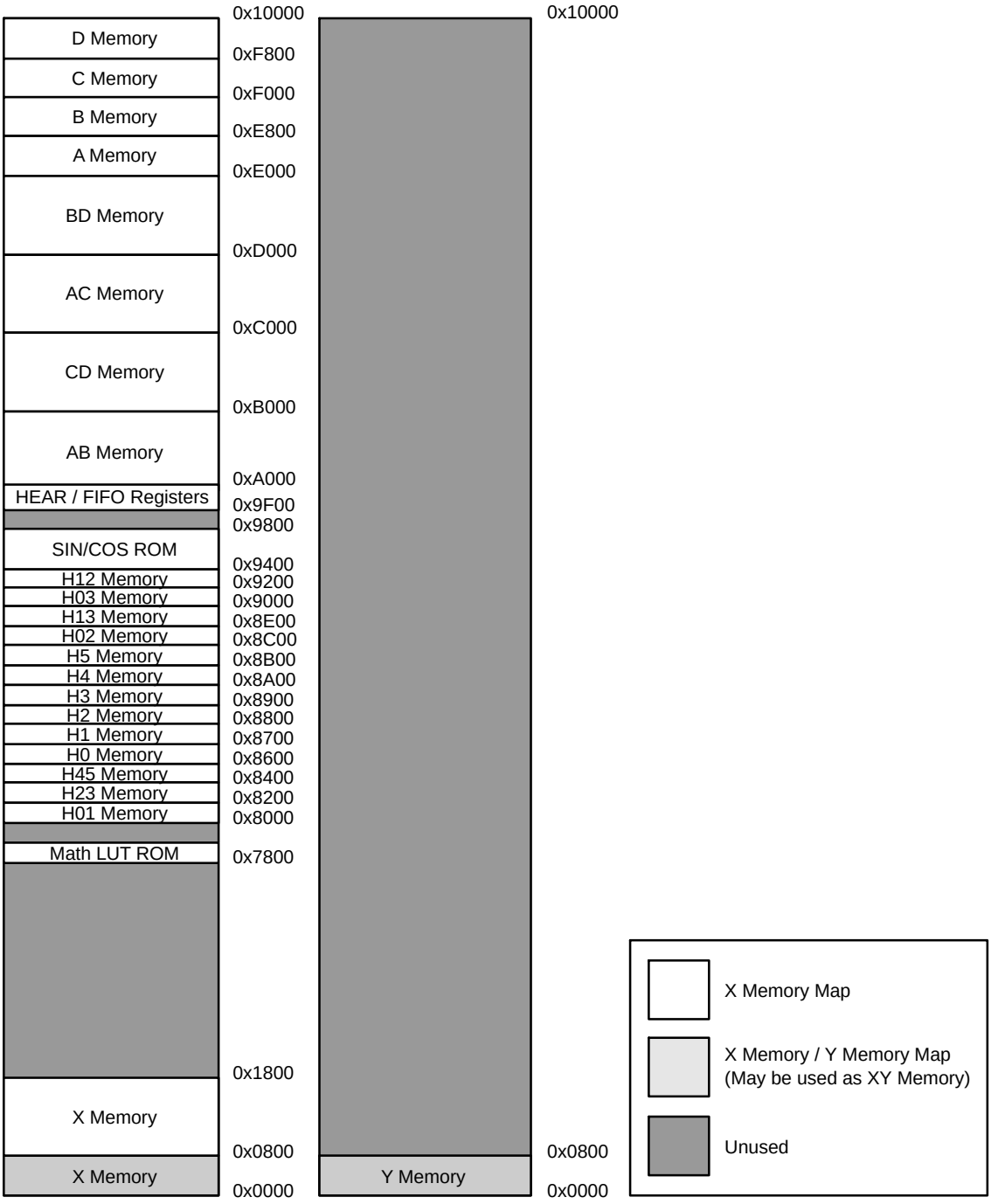


Figure 5. XMEM and YMEM Memory Maps

The structure of the PMEM address space is shown in Figure 6.

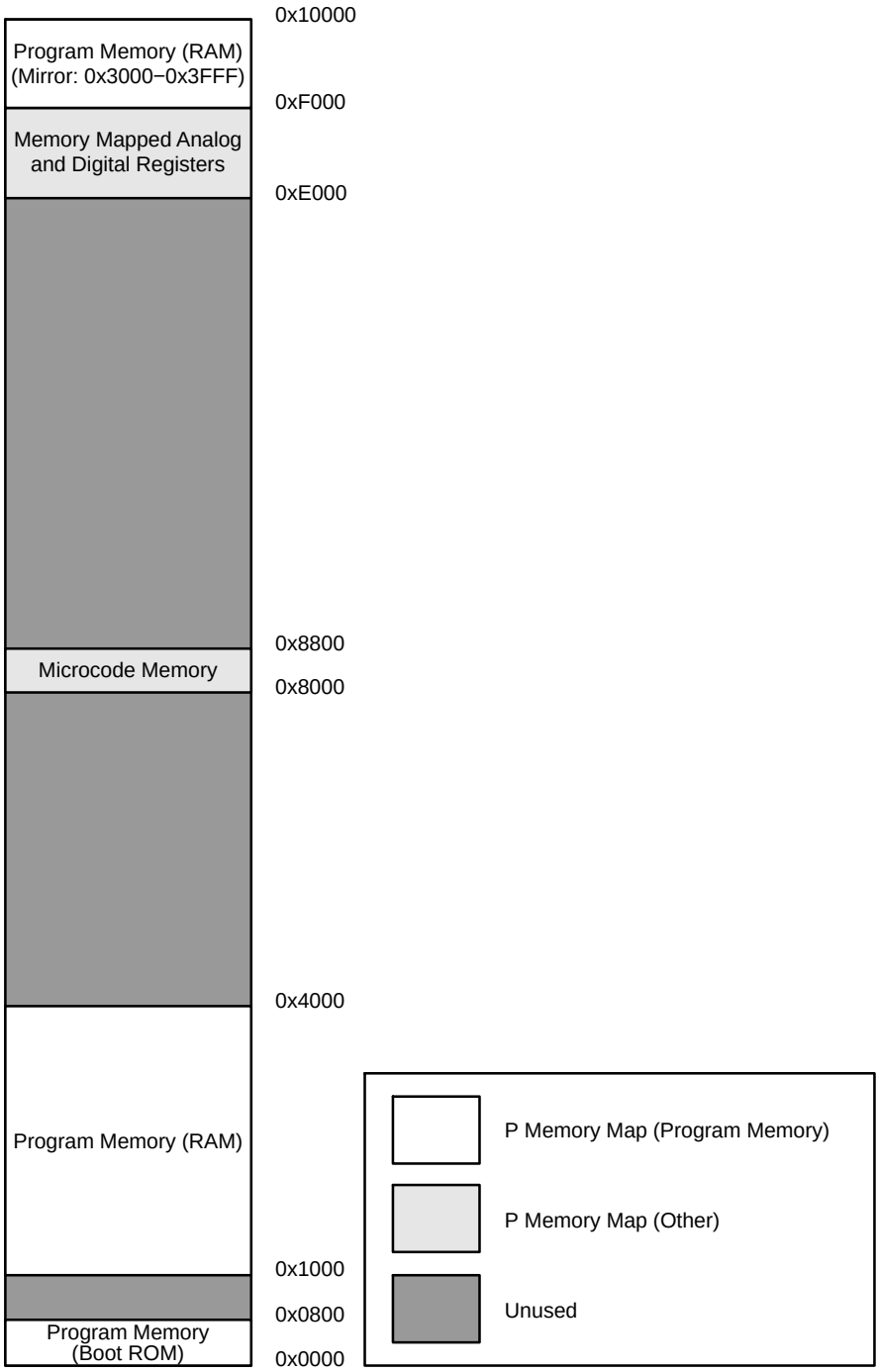


Figure 6. PMEM Memory Map

Other Digital Blocks and Functions

General−Purpose Timer

The CFX DSP system contains two general−purpose timers. These can be used for scheduling tasks that are not part of the sample−based signal−processing scheme, such as checking the battery voltage, and periodically asserting the available analog and digital inputs for purposes such as reading the value of a volume control potentiometer or detecting input from a push button.

Watchdog Timer

The watchdog timer is a programmable hardware timer that operates from the system clock and is used to ensure system sanity. It is always active and must be periodically acknowledged as a check that an application is still running. Once the watchdog times out, it generates an interrupt. If left to time out a second consecutive time without acknowledgement, a system reset will occur.

Interrupts

The interrupt flow of the system handles interrupts generated by the CFX DSP core and the HEAR accelerator. The CFX interrupt controller receives interrupts from the various blocks within the system. The FIFO controller can send interrupts to the CFX. The HEAR can generate events which are interrupts in the CFX.

Hear Function Chain Controller

The HEAR function chain controller responds to commands from the CFX, and events from the FIFO controller. It must be configured by the CFX to enable the triggering of particular function chains within a microcode configuration. This is accomplished through the appropriate setting of control registers as described in the Hardware Reference Manual for BelaSigna 300.

The interaction between the interrupt controller, the HEAR function chain controller and the rest of the system are shown in Figure 7.

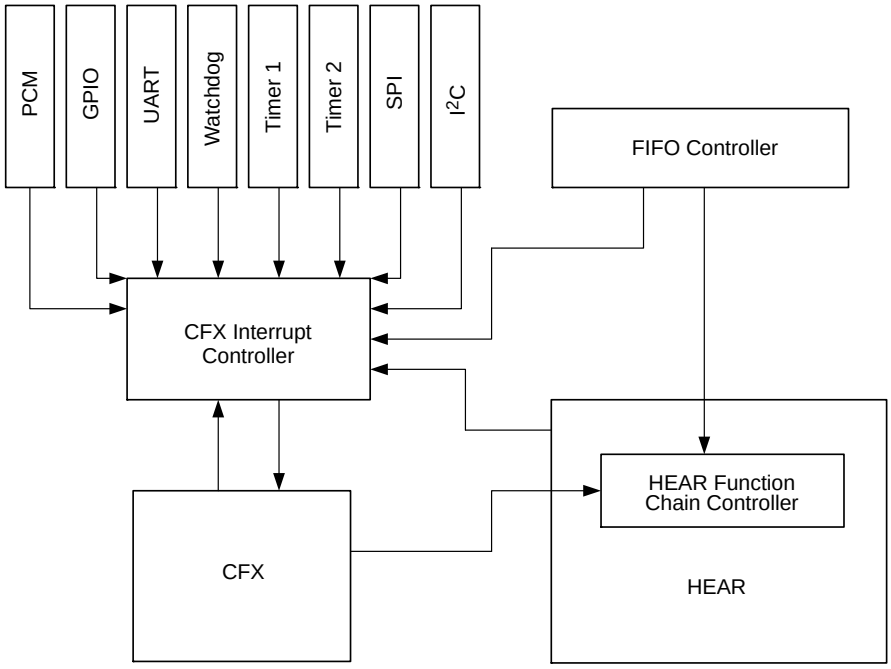


Figure 7. Interrupt Flow

Algorithm and Data Security

Algorithm software code and user data that requires permanent retention is stored off the BelaSigna 300 chip in separate non−volatile memory. To support this, the BelaSigna 300 chip can gluelessly interface to an external SPI EEPROM.

To prevent unauthorized access to the sensitive intellectual property (IP) stored in the EEPROM, a comprehensive system is in place to protect manufacturer's application code and data. When locked the system implements an access restriction layer that prevents access to both volatile and non−volatile system memory. When unlocked, both memory and EEPROM are accessible.

To protect the IP in the non−volatile memory the system supports decoding algorithm and data sections belonging to an application that have been encrypted using the advanced encryption standard (AES) and stored in non−volatile memory. While system access restrictions are in place, the keys used in the decryption of these sections will be secured from external access by the regular access restrictions. When the system is externally "unlocked" these keys will be cleared, preventing their use in decoding an application by non−authorized parties. After un−restricting access in this way the system may then be restored by re−programming the decryption keys.

Analog Blocks

Input Stage

The analog audio input stage is comprised of four individual channels. For each channel, one input can be selected from any of the five possible input sources (depending on package option) and is then routed to the input of the programmable preamplifier that can be configured for bypass or gain values of 12 to 30 dB (3 dB steps). The input stage is shown in Figure 8.

A built−in feature allows a sampling delay to be configured for any one or more channels. This is useful in beam−forming applications.

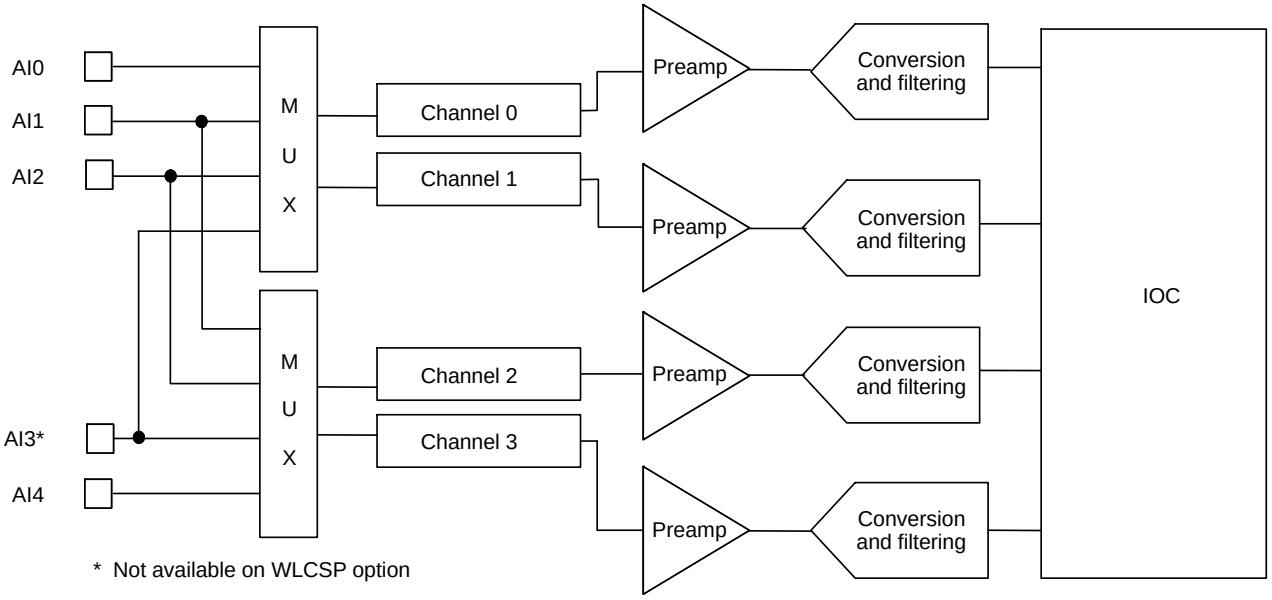


Figure 8. Input Stage

Input Dynamic Range Extension (IDRX)

To increase the input dynamic range for a particular application, it is possible to pair−wise combine the four AD converters found on BelaSigna 300. This will increase the dynamic range up to 110 dB. When this technique is used, the device handles the preamplifier gain configuration based on the input level and sets it in such a way as to give the maximum possible dynamic range. This avoids having to make the design trade−off between sufficient amplification for low−level signals and avoiding saturation for high−level signals.

Output Stage

The output stage includes a 3rd−order sigma−delta modulator to produce a pulse density modulated (PDM) output signal. The sampling frequency of the sigma delta modulator is pre−scaled from the system clock.

The low−impedance output driver can also be used to directly drive an output transducer without the need for a separate power amplifier or can be connected to another Digital Mic input on another system. The output stage is shown in Figure 9.

BelaSigna 300 has an option for high−power mode that decreases the impedance of the output stage, thus permitting higher possible acoustic output levels. To use this feature, RCVR_HP+ should be connected to RCVR+, and RCVR_HP− should be connected to RCVR−, you must combine the synchronized output signals externally to BelaSigna 300. Connect both RCVR+ and RCVR_HP+ to a single terminal on an output transducer, and connect both RCVR− and RCVR_HP− to the other terminal. An RC filter might be required based on receiver characteristics. Figure 9 shows the connections for the output driver in high−power mode.

Electrical specifications on the output stage are available in Table 2.

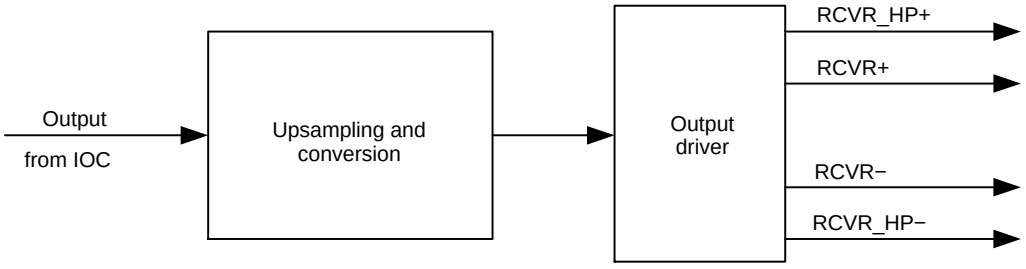


Figure 9. Output Stage

Figure 10. External Signal Routing of Connections for High−Power Output Mode

The high−frequencies in the Class−D PDM output are filtered by an RC filter or by the frequency response of the speaker itself. ON Semiconductor recommends a 2−pole RC filter on the output stage if the output signal is not directly driving a receiver. Given below is the simple schematic for a 2−pole RC filter.

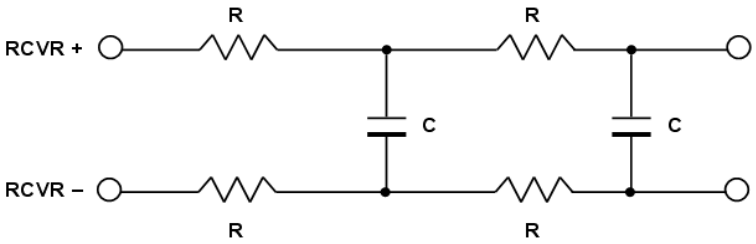


Figure 11. 2−Pole RC filter

Our recommendations for components for the RC Filter are given below:

For 8 KHz sampling, we recommend R = 8.2 k and C = 1 nF (3 dB cutoff frequency at 3.3 kHz)

For 16 KHz sampling, we recommend R = 8.2 k and C = 330 pF (3 dB cutoff frequency at 9 kHz)

Clock Generation Circuitry

BelaSigna 300 is equipped with an un−calibrated internal RC oscillator that will provide clock support for booting and stand−by mode operations. This internal clocking circuitry cannot be used during normal operation; as such, an external clock signal must be present on the EXT_CLK pin to allow BelaSigna 300 to operate. All other needed clocks in the system are derived from this external clock frequency. Figure 12 shows the internal clock structure of BelaSigna 300.

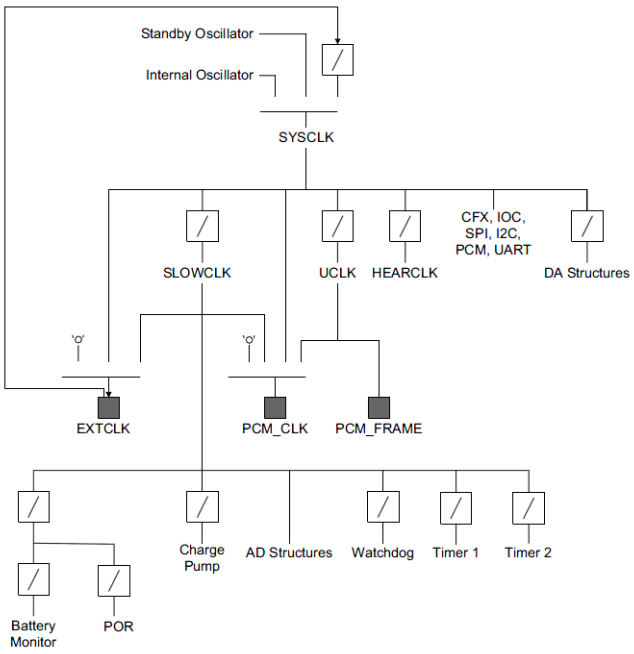


Figure 12. Internal Clocking Structure

Power Supply Unit

BelaSigna 300 has multiple power sources as can be seen on Figure 13. Digital and analog sections of the chip have their own power supplies to allow exceptional audio quality.

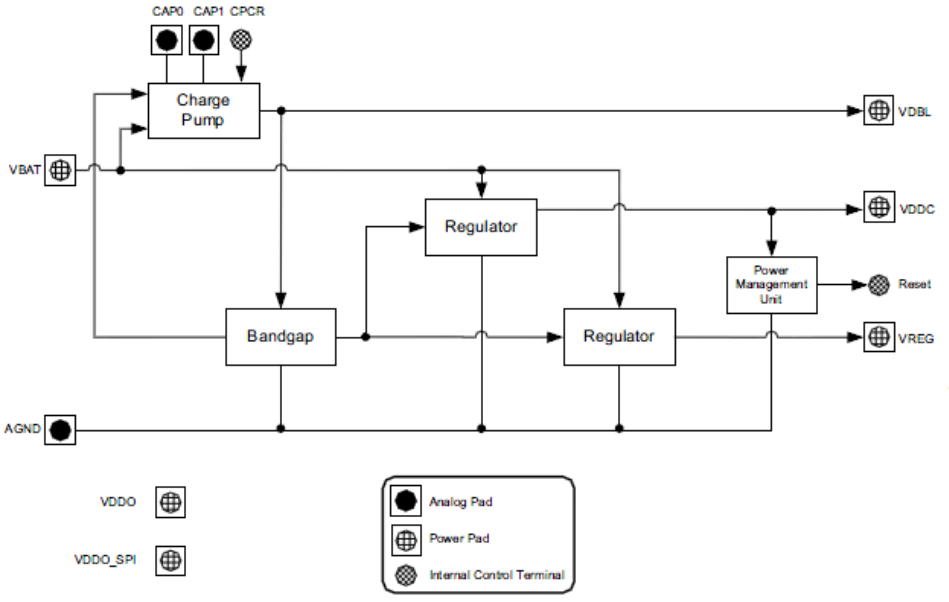


Figure 13. Power Supply Structure

Battery Supply Voltage (VBAT)

The primary voltage supplied to a BelaSigna 300 device is VBAT. It is typically 1.8 V. BelaSigna 300 also uses VBAT to define the I/O voltage levels, as well as powering an external EEPROM on the SPI port. Consequently, any voltage below 1.8 V will result in incorrect operation of the EEPROM.

Internal Band Gap Reference Voltage

The band gap reference voltage has been stabilized over temperature and process variations. This reference voltage is used in the generation of all of the regulated voltages in the BelaSigna 300 system and provides a nominal 1 V reference signal to all components using the reference voltage.

Internal Digital Supply Voltage (VDDC)

The internal digital supply voltage is used as the supply voltage for all internal digital components, including being used as the interface voltage at the low side of the level translation circuitry attached to all of the external digital pads. VDDC is also provided as an output pad, where a capacitor to ground typically filters power supply noise. The VDDC internal regulator is a programmable power supply that allows the selection of the lowest digital supply depending on the clock frequency at which BelaSigna 300 will operate. In BelaSigna 300, the VDDC configuration is set by the boot ROM to its maximum value to allow for 40 MHz operation in all parts. Contact ON Semiconductor for more information regarding VDDC calibration.

External Digital Supply Voltage (VDDO)

This pin is not available on BelaSigna 300, as it is internally connected to VBAT.

SPI Port Digital Supply Voltage (VDDO_SPI)

VDDO_SPI is an externally provided power source dedicated to the SPI port. Communication with external EEPROMs will happen at the level defined on this pin. This pin is not available on the WLCSP option of BelaSigna 300, as it is internally connected to VBAT.

Regulated Supply Voltage (VREG)

VREG is a 1 V reference to the analog circuitry. It is available externally to allow for additional noise filtering of the regulated voltages within the system.

Regulated Doubled Supply Voltage (VDBL)

VDBL is a 2 V reference voltage generated from the internal charge pump. It is a reference to the analog circuitry. It is available externally to allow for additional noise filtering of the regulated voltages within the system.

The internal charge pump uses an external capacitor that is periodically refreshed to maintain the 2 V supply. The charge pump refresh frequency is derived from slow clock which assists the input stage in filtering out any noise generated by the dynamic current draw on this supply voltage.

Voltage Mode

BelaSigna 300 operates in: **Low voltage (LV) power supply mode**. This mode allows integration into a wide variety of devices with a range of voltage supplies and communications levels. BelaSigna 300 operates from a nominal supply of 1.8 V on VBAT, but this can scale depending on available supply. The digital logic runs on an internally generated regulated voltage (VDDC), in the range of 0.9 V to 1.2 V. On the WLCSP package option, all digital I/O pads including the SPI port run from the same voltage as supplied on VBAT.

The power management on BelaSigna 300 includes the power−on−reset (POR) functionality as well as power supervisory circuitry. These two components work together to ensure proper device operation under all battery conditions.

The power supervisory circuitry monitors both the battery supply voltage (VBAT) and the internal digital supply voltage (VDDC). This circuit is used to start the system when VBAT reaches a safe startup voltage, and to reset the system when either of the VBAT or VDDC voltages drops below a relevant voltage threshold. The relevant threshold voltages are shown in Table 12.

Table 12. POWER MANAGEMENT THRESHOLDS

Threshold	Voltage Level
VBAT monitor startup	0.70 V
VBAT startup	0.82 V ± 50 mV
VBAT and VDDC shutdown	0.80 V ± 50 mV

Power−on−Reset (POR) and Booting Sequence

BelaSigna 300 uses a POR sequence to ensure proper system behavior during start−up and proper system configuration after start−up. At the start of the POR sequence, the audio output is disabled and all configuration and control registers are asynchronously reset to their default values (as specified in the Hardware Reference Manual for BelaSigna 300). All CFX DSP registers are cleared and the contents of all RAM instances are unspecified at this point.

The POR sequence consists of two phases: voltage supply stabilization and boot ROM initialization. During the voltage supply stabilization phase, the following steps are performed:

1. The internal regulators are enabled and allowed to stabilize.
2. The internal charge pump is enabled and allowed to stabilize.
3. SYSCLK is connected to all of the system components.
4. The system switches to external clocking mode

Power Management Strategy

BelaSigna 300 has a built−in power management unit that guarantees valid system operation under any voltage supply condition to prevent any unexpected audio output as the result of any supply irregularity. The unit constantly monitors the power supply and shuts down all functional units (including all units in the audio path) when the power supply voltage goes below a level at which point valid operation can no longer be guaranteed.

Once the supply voltage rises above the startup voltage of the internal regulator that supplies the digital subsystems ($VDDC_{STARTUP}$) and remains there for the length of time T_{POR}, a POR will occur. If the supply is consistent, the internal system voltage will then remain at a fixed nominal voltage ($VDDC_{NOMINAL}$). If a spike occurs that causes the voltage to drop below the shutdown internal system voltage ($VDDC_{SHUTDOWN}$), the system will shut down. If the voltage rises again above the startup voltage and remains there for the length of time T_{POR}, a POR will occur. If

operating directly off a battery, the system will not power down until the voltage drops below the $VDDC_{SHUTDOWN}$ voltage as the battery dies. This prevents unwanted resets when the voltage is just on the edge of being too low for the system to operate properly because the difference between $VDDC_{STARTUP}$ and $VDDC_{SHUTDOWN}$ prevents oscillation around the $VDDC_{SHUTDOWN}$ point.

Other Analog Support Blocks and Functions

Low−Speed A/D Converters (LSAD)

The BelaSigna 300 chip has four LSAD channels that connect to external analog inputs for purposes such as for reading the value of a potentiometer or an analog sensor (LSAD[1..4]). The native data format for the LSAD is 10−bit two's−complement. However, a total of eight operation modes are provided that allow a configurable input dynamic range in cases where certain minimum and maximum values for the converted inputs are desired, such as in the case of a volume control where only input values up to a certain magnitude are allowed. Each LSAD channel is sampled at a nominal frequency of 1.6 kHz when using the default settings. Each LSAD pin is multiplexed with a GPIO function (see the General−Purpose Input Output Ports section) as such the functionality of the pin can be either a GPIO or an LSAD depending on the configuration.

Battery Monitor

A programmable on−chip battery monitor is available for overall system power management. The battery monitor works by incrementing a counter value every time the battery voltage goes below a desired, configurable threshold value. This counter value can be used in an application−specific power−management algorithm running on the CFX. The CFX can initiate any desired actions once the battery hits a predetermined value.

Digital Interfaces

General−Purpose Input Output (GPIO) Ports

BelaSigna 300 has five GPIO ports that can connect to external digital inputs such as push buttons, or digital outputs such as the control or trigger of an external companion chip (GPIO[0..4]). The direction of these ports (input or output) is configurable and each pin has an internal pull−up resistor when configured as a GPIO. A read from an unconnected pin will give a value of logic 1. Four of the five GPIO pins are multiplexed with an LSAD (see the Low−Speed A.D Converters section) and as such the functionality of the pin can be either a GPIO or an LSAD depending on the configuration. Note that GPIO0 cannot be used as an LSAD.

Inter−IC Communication (I^2C) Interfaces

The I^2C interface is an industry−standard interface that can be used for high−speed transmission of data between BelaSigna 300 and an external device. The interface operates at speeds up to 400 Kbit/sec for system clocks (EXT_CLK) higher than 1.6 MHz. In product development mode, the I^2C interface is used for application debugging purposes, communicating with the BelaSigna 300 development tools. The interface can be configured to operate in either master mode or slave mode.

Serial Peripheral Interface (SPI) Port

An SPI port is available on BelaSigna 300 for applications such as communication with a non−volatile memory (EEPROM). The I/O levels on this port are defined by the voltage on the VDDO_SPI pin on the DFN package option, whereas it is defined by VBAT on the WLCSP package option. The SPI port operates in master mode only, which supports communications with slave SPI devices.

The SPI port on BelaSigna 300 only supports master mode, so it will only communicate with SPI slave devices. When connecting to an SPI slave device other than a boot EEPROM, the SPI_CS pin should be left unconnected and the slave device CS line should be driven from a GPIO to avoid BelaSigna 300 boot malfunction. When connecting to an SPI EEPROM for boot, the designer can choose to connect the SPI_CS pin to the EEPROM or use a GPIO (high at boot) for a design with several daisy-chained SPI devices.

PCM Interface

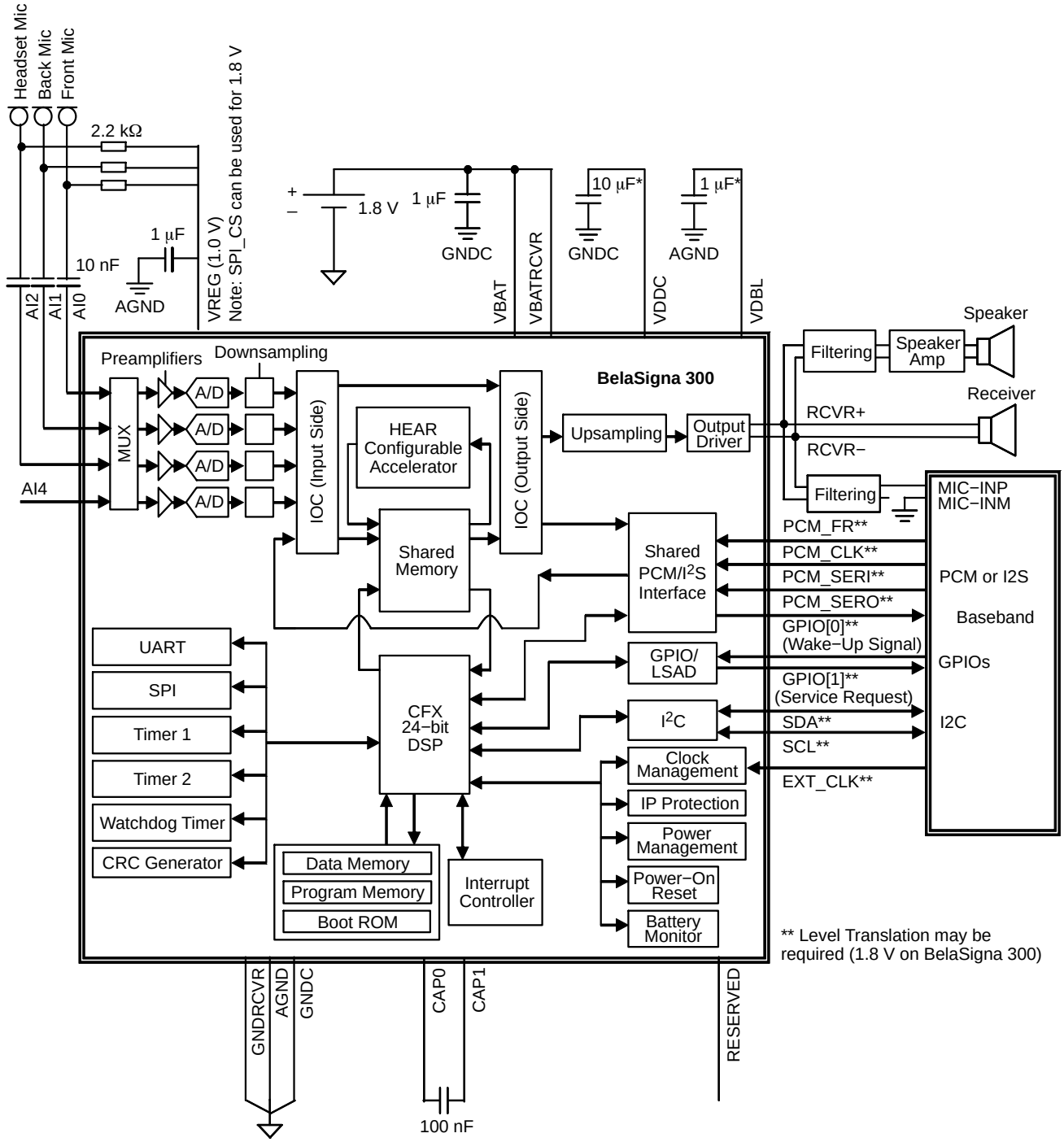
BelaSigna 300 includes a highly configurable pulse code modulation (PCM) interface that can be used to stream signal, control and configuration data into and out of the device. The I/O levels on this port are defined by the voltage on the VBAT pin.

UART Interface

A general−purpose two−pin UART interface is available for RS−232 compatible communications. The baud rate (bits/second) of this interface is typically configurable within a range of 0.4 to 320 kbps, depending on the application's system clock. The I/O levels on this port are defined by the voltage on the VBAT pin.

Application Diagrams

The application diagram of BelaSigna 300 is shown in Figure 14.



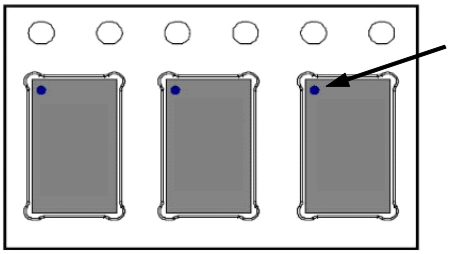
*The VDDC and VDBL capacitor values shown are the recommended values for current production parts (B300W35A109XXG and B300D44A103XXG).
For parts manufactured before January 1st, 2015 (B300W35A102XYG and B300D44102XXG, or parts with a Date Code earlier than "1501"), it is recommended that the value of the VDBL capacitor be at least the same value as the VDDC capacitor, and should ideally be double the value. The recommended VDDC and VDBL capacitor values for these older parts are a VDDC capacitor of 10 μF and a VDBL capacitor of 20 μF. For more information contact your ON Semiconductor support representative.

Figure 14. BelaSigna 300 Application Diagram

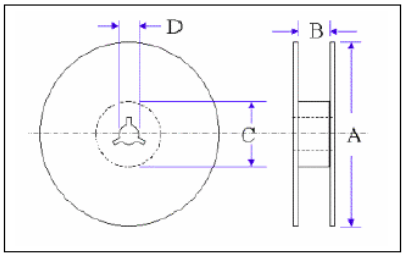
Assembly Information

CARRIER DETAILS
2.6 x 3.8 mm WLCSP

ON Semiconductor offers tape and reel packing for BelaSigna 300. The packing consists of a pocketed carrier tape, a cover tape, and a molded anti−static polystyrene reel. The carrier and cover tape create an ESD safe environment, protecting the components from physical and electrostatic damage during shipping and handling.

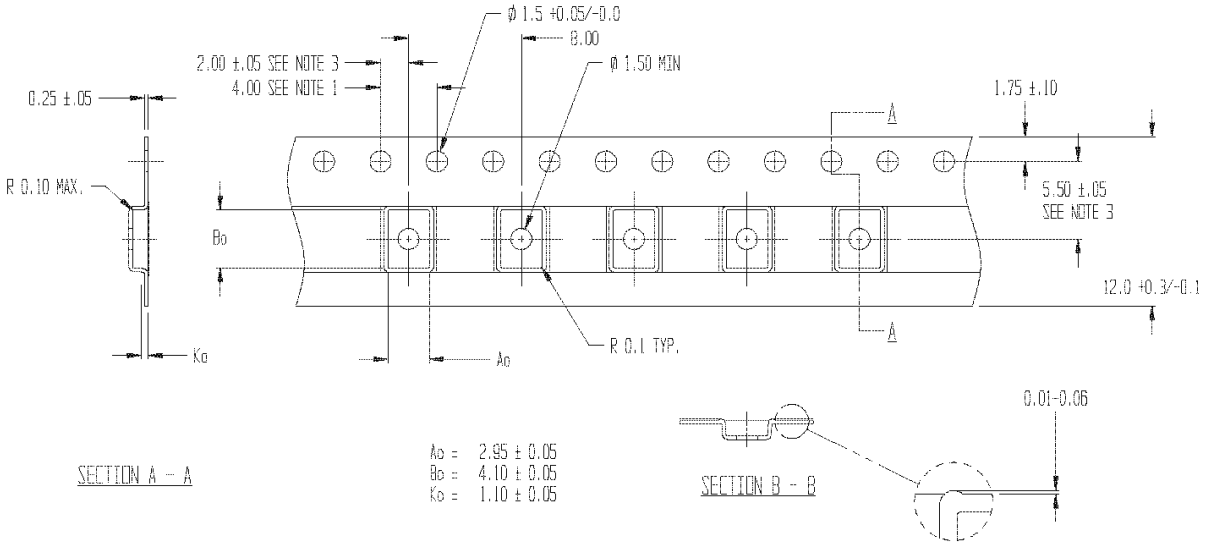


Quantity per Reel: 2500 units
Pin 1 Orientation: Upper Left, Bumps down
Tape Brand / Width: Advantek / 12 mm
Pocket Pitch: 8 mm
P/N: BCB043
Cover Tape: 3M 2666 PSA 9.3 mm



A = 13 inches
B = 12 mm
C = 4 inches
D = 13 mm
Reel Brand / Width: Advantek Lokreel® / 13 in

Figure 15. Package Orientation on Tape



10 sprockets hole pitch cumulative tolerance ±0.1.
Camber in compliance with EIA 763.
Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Figure 16. Carrier Tape Drawing

Sample Shipping Label

Figure 17. Sample Shipping Label

Re−Flow Information

The re−flow profile depends on the equipment that is used for the re−flow and the assembly that is being re−flowed. Information from JEDEC Standard 22−A113D and J−STD−020D.01 can be used as a guideline.

Electrostatic Discharge (ESD) Sensitive Device

CAUTION: ESD sensitive device. Permanent damage may occur on devices subjected to high−energy electrostatic discharges. Proper ESD precautions in handling, packaging and testing are recommended to avoid performance degradation or loss of functionality. Device is 2 kV HBM ESD qualified.

Miscellaneous

Ordering Information

To order BelaSigna 300, please contact your account manager and ask for part number B300W35A109XXG.

Chip Identification

Chip identification information can be retrieved by using the Communications Accelerator Adaptor (CAA) tool along with the protocol software provided by ON Semiconductor (see CAA instruction manual). For BelaSigna 300, the key identifier components and values are as follows:

Chip Family	Chip Version	Chip Revision
0x03	0x02	0x0100

Support Software

A full suite of comprehensive tools is available to assist software developers from the initial concept and technology assessment through to prototyping and product launch. Simulation, application development and communication tools as well as an Evaluation and Development Kit (EDK) facilitate the development of advanced algorithms on BelaSigna 300.

Training

To facilitate development on the BelaSigna 300 platform, training is available upon request. Contact your account manager for more information.

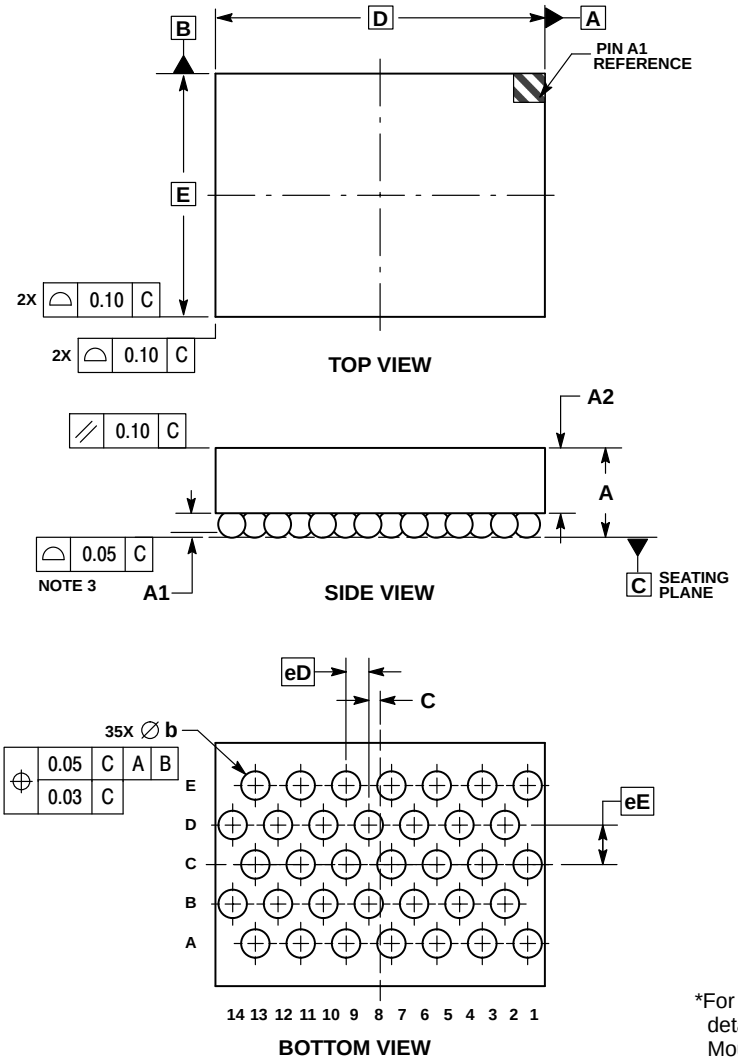
Company or Product Inquiries

For more information about ON Semiconductor products or services visit our Web site at http://onsemi.com.

BelaSigna 300

PACKAGE DIMENSIONS

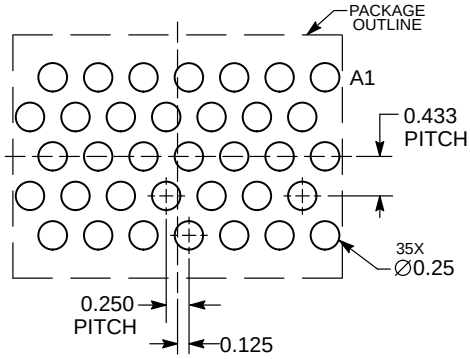
WLCSP35, 3.63x2.68
CASE 567AG
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.84	1.00
A1	0.17	0.23
A2	0.72 REF	
b	0.24	0.29
C	0.125 BSC	
D	3.63 BSC	
E	2.68 BSC	
eD	0.25 BSC	
eE	0.433 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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